IN THE CLAIMS

Please amend the claims as follows:

Claims 1-22 (Canceled).

23. (Currently Amended) An integrated circuit comprising:

a color sensor array having a plurality of sensor elements of different first and second colors, arranged in rows and columns;

a first reset shift register having a plurality of outputs, each output being coupled to control a reset of sensor elements of the first color that are in a respective one of the rows of the array;

a second reset shift register having a plurality of outputs, each output being coupled to control a reset of sensor elements of the second color that are in a respective one of the rows of the array;

a wordline shift register having a plurality of outputs, each output being coupled to control a readout of the sensor elements that are in a respective one of the rows of the array; and

control logic coupled to feed (a) each of the first and second shift registers with ~~a pair of reset bits~~ a first reset bit and a second reset bit and (b) the wordline shift register with a read bit, and to operate the reset and wordline shift registers so that the ~~pair of~~first and second reset bits and the read bit shift through their respective registers while an image frame is being captured, with ~~one of the reset bits of said pair~~the first reset bit ~~always~~ being one or more rows ahead of the read bit to mark the start of integration, and the ~~other one of said pair~~second reset bit to generate a correlated double sampling pixel reset value after each pixel integrated intensity value, and wherein ~~the control logic is to program the reset bits of said pair to set the integration time independently for the first and second colors~~ integration time for first color and second color can be set independently by using the control logic to control timing of the first reset bit fed to each of the first and second reset shift registers.

24. (Previously Presented) The integrated circuit of claim 23 wherein the plurality of sensor elements of the color sensor array are of red, green, and blue colors, the first color being red and the second color being green.

25. (Currently Amended) The integrated circuit of claim 24 wherein the plurality of sensor elements are CMOS active pixel elements with an RGB color filter array that has a Bayer pattern, the sensor array having less than or equal to two reset metal lines for each row that are coupled to a respective pair of outputs of the first and second registers.

26. (Previously Presented) The integrated circuit of claim 23 further comprising a third reset shift register having a plurality of outputs, each output being coupled to control a reset of sensor elements of a third color, wherein the control logic is further coupled to feed the third reset shift register with only one reset bit, and wherein the sensor elements whose reset is controlled by the third reset shift register have the longest integration time of the array.

27. (Currently Amended) A system comprising:

a color sensor array having a plurality of sensor elements of different first and second colors, arranged in rows and columns, the elements of each column being coupled to share a respective one of a plurality of bitlines of the array;

a first reset shift register having a plurality of outputs, each output being coupled to control a reset of sensor elements of the first color that are in a respective one of the rows of the array;

a second reset shift register having a plurality of outputs, each output being coupled to control a reset of sensor elements of the second color that are in a respective one of the rows of the array;

a wordline shift register having a plurality of outputs, each output being coupled to control a readout of the sensor elements that are in a respective one of the rows of the array;

control logic coupled to feed (a) each of the first and second registers with ~~a pair of reset bits~~ a first reset bit and a second reset bit and (b) the wordline shift register with a read bit, and to operate the reset and wordline shift registers so that the ~~pair of~~first and second reset bits and the read bit shift through their respective registers while an image frame is being captured, with ~~one~~

~~of the reset bits~~the first reset bit ~~always~~ being one or more rows ahead the read bit to mark the start of integration, and the ~~other one of said pair~~second reset bit to generate a pixel reset level after each pixel integrated intensity level generated by the read bit, and wherein ~~the control logic is to program the reset bits of said pair to set the integration time independently for the first and second colors.~~ the start of integration for the sensor elements of each color can differ by controlling timing of the first reset bit fed to each of the first and second reset shift registers;

signal and image processing circuitry coupled to the plurality of bitlines to digitize pixel levels produced by the sensor array;

a system controller coupled to control the sensor array and control logic so that pixel levels are read from the array one row at a time in accordance with the read bit, the controller being further coupled to control the signal and image processing circuitry to enable formation of a digital image file;

a host computer interface coupled to the system controller to pass the digital image file to a host computer; and

a local user interface of the system, being coupled to the system controller.

28. (Previously Presented) The system of claim 27 wherein the plurality of sensor elements of the color sensor array are of red, green, and blue colors, the first color being red and the second color being green.

29. (Previously Presented) The system of claim 28 wherein the plurality of sensor elements are CMOS active pixel elements with an RGB color filter array that has a Bayer pattern, the sensor array having two reset metal lines for each row that are coupled to a respective pair of outputs of the first and second registers.

30. (Previously Presented) The system of claim 27 further comprising a third reset shift register having a plurality of outputs, each output being coupled to control a reset of sensor elements of a third color, wherein the control logic is further coupled to feed the third reset shift register with only one reset bit, and wherein the sensor elements whose reset is controlled by the third reset shift register have the longest integration time of the array.

Please add the following new claims:

31. (New) An integrated circuit comprising:

a color sensor array having a plurality of sensor elements of first color, second color and third color, arranged in rows and columns;

a first reset shift register having a plurality of outputs, each output being coupled to control a reset of sensor elements of the first color;

a second reset shift register having a plurality of outputs, each output being coupled to control a reset of sensor elements of the second color;

a third reset shift register having a plurality of outputs, each output being coupled to control a reset of sensor elements of the third color;

a readout shift register having a plurality of outputs, each output being coupled to control a readout of the sensor elements; and

control logic coupled to each of the shift registers and the readout shift register, the control logic to control the reset shift registers and the readout shift register such that charge accumulation levels of the sensors elements of each of the three colors can be set independently, wherein the color sensor array has less than or equal to two reset metal lines for each row of the sensor elements to receive reset signals from the reset shift registers.

32. (New) The integrated circuit of claim 31, wherein start of integration for the sensor elements of each color can differ by controlling timing of a rest signal sent to each of the reset shift register.

33. (New) The integrated circuit of claim 31, wherein the control logic feeds each of the reset shift registers with a pair of reset signals and the readout shift register with a read signal.

34. (New) The integrated circuit of claim 33, wherein the control logic operates the reset shift registers and readout shift registers so that the pair of reset signals and the read signal shift through their respective registers while an image frame is being captured.

35. (New) The integrated circuit of claim 34, wherein one of the reset signals is one or more rows ahead of the read signal to mark the start of integration, and the other one of the reset signals is used to generate a correlated double sampling pixel reset value after each pixel integrated intensity value.